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Gold-coated porous silicon films as anodes for lithium ion batteries

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ABSTRACT

Silicon has the highest known theoretical charge capacity for lithium, making it a promising material for rechargeable lithium ion batteries (LIB). A significant drawback of silicon anodes is the large volume change associated with the insertion and extraction of lithium, which oftentimes leads to cracking and pulverization of the anode, limiting its cycle life. We present a layered architecture consisting of a gold-coated porous silicon film attached to a bulk silicon substrate. This structure demonstrates an enhanced ability to alloy with lithium ions over several charge/discharge cycles while maintaining mechanical integrity. With this structure we show that a specific capacity of over 3000 mAh g^{-1} can be achieved for over 50 charge–discharge cycles at 100 μA cm^{-2}, and 2500 mAh g^{-1} can be achieved for over 75 cycles with coulombic efficiencies over 95%. This is a significant improvement over a gold-coated, non-porous silicon sample, which had a maximum capacity of 1 mAh g^{-1} before failing after 10 cycles at 0.25 mAh g^{-1} when cycled at a constant current of 100 μA cm^{-2}, illustrating the benefit of internal pores. Gold-coated porous silicon out-performed non-gold-coated porous silicon, which had a first cycle discharge capacities of 500 mAh g^{-1}, which quickly faded to 76 mAh g^{-1} after the 10th cycle when cycled at a constant current of 50 μA cm^{-2}. The combination of internal pores and a gold-coating points to a new approach to improving the long-term cycleability and high-capacity performance metrics of LIB anodes.

1. Introduction

The development of lightweight, long lasting lithium ion batteries continues to be of great technological importance because of their increasing use in portable electronics, computing, and telecommunications [1,2]. Lithium ion batteries are also used in plug-in hybrid vehicles, power tools, aerospace and power grid applications [3,4]. Developing new electrodes with higher capacity or higher energy density remains one of the most important areas in lithium ion battery research.

Presently, carbon-based materials (e.g. graphite) are utilized as the anode material in most rechargeable batteries [5,6]. At room temperature, the highest achievable specific capacity for silicon is 3579 mAh g^{-1}, far greater than the theoretical capacity of 372 mAh g^{-1} for graphite [7,8]. However, silicon is encumbered with a ~300% volumetric change during insertion and extraction of lithium ions [9,10]. This leads to cracking and pulverization of the silicon electrode, causing loss of electrical contact and rapid fading of capacity.

A variety of silicon structures and silicon-based composites have been examined in order to reduce the lithiation-induced stress and suppress the structural destruction of silicon, which is believed to be the main cause for the capacity decrease during charge/discharge cycling [1,9,11–18]. Examples include the use of pure Si micro- and nanoscale particle anodes, Si dispersed in an active/inactive matrix, Si mixed with different binders, and both amorphous and crystalline Si thin films. Other nanostructured silicon including three-dimensional porous Si particles [16], Si nanowires [19], Si core–shell nanowires [20], microstructured nanopore-walled porous silicon [21,22] and Si nanosprings [23], have demonstrated improved capacities and cycleability over bulk Si. However, it should be noted that most studies with nanostructured Si electrodes in Li ion batteries have been limited to 100 or fewer charge–discharge cycles. Many of these structures also require difficult or expensive processing steps, limiting their potential for commercialization. Additionally, recently it has been shown that thin metal coatings such as silver [24] can increase the capacity and cycle life of silicon materials. Arie and coworkers have shown that a 100 nm film of fullerene molecules on an evaporated silicon film is able to stabilize the material [25]. They attribute the increase in electrochemical performance to a stable SEI layer that did not increase in thickness as the material was cycled. However many of these studies have not combined these thin films with

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silicon structuring. Additionally, in thin film silicon geometries, there has been little description of the role of the underlying support structure. Here we combine a porous silicon architecture attached to a bulk silicon substrate with a thin gold coating to achieve the benefits of both structuring and the metal coating.

In lithium ion batteries, lithium ions are de-intercalated from the anode material during discharge, transported through an electrolyte filled micro-porous separator and reinserted into the cathode material. Electrons are transferred through an external circuit, delivering electric energy to the device. One important parameter of the anode material is its specific capacity because it impacts the energy density of the battery. Another important parameter is cycleability, which is the number of times the material can intercalate and de-intercalate lithium ions without significant degradation or significant loss of capacity. This parameter will directly influence the performance and cycle life of the battery. For our gold-coated porous silicon materials, we report excellent cyclic stability: a capacity that is 70% of theoretical capacity for 100 cycles with coulombic efficiencies between 97 and 99%. We suggest that the extended cycle life of this material originates with the unique micromechanical properties of the hybrid gold-porous silicon layer.

2. Experimental

2.1. Porous silicon preparation

Prime grade, boron doped, p-type (1 0 0) silicon wafers (Siltronix Corp) were used. The wafer presented has a thickness of 300 μm measured using profilometry (Dektak 32, Veeco Instruments) with an average resistivity between 14 and 22 Ω-cm as reported by the supplier. Porous silicon electrodes were prepared by electrochemically etching pores into the silicon wafer. A cylindrical teflon cell is used with a hydrofluoric acid (HF) etch solution. The cell contains an aluminum plate connected to a power supply (Agilent E3612A DC Power Supply), a Viton gasket that defines the region to be etched, and a platinum wire counter electrode. The backside of the wafer is coated with aluminum to reduce the contact resistance with the aluminum back plate. The etching solution is composed of 25 mL dimethylformamide (DMF, Sigma Aldrich) and 2 mL 49% HF (Fisher Scientific) solution. The etching is performed at 8 mA in a 5 cm^2 etch cell for 120 min. The wafer is then removed from the electrochemical etch cell and then placed in an HF bath for 1 min to remove the backside aluminum layer. A scanning electron microscopy (SEM, FEI Quanta 400) image of a representative porous silicon sample containing pores with an average diameter of 1 micron, an average depth of 5.5 microns, and a porous silicon mass of 0.78 mg is shown in Fig. 1a and b.

2.2. Mass of porous silicon

The mass of the active layer is taken to be the mass of the porous silicon. As will be discussed in Section 3, characterization of the material after cycling indicates that the bulk silicon layer does not contribute significantly to the cycling with lithium. The active mass of the silicon is calculated from the porosity and thickness of the porous silicon layer. The porosity is defined as the fraction of void within the porous silicon layer and can be determined easily by gravimetric measurements [26]. The porosity is simply given by:

$$P(\%) = \frac{m_1 - m_2}{m_1 - m_3} \quad (1)$$

where m_1 is the mass of the wafer before etching, m_2 is the mass after etching, and m_3 is the mass of the bulk silicon beneath the porous silicon. Therefore, the difference between m_1 and m_3 will result in the mass of the porous silicon.

This difference is also related to the thickness of the porous silicon layer via the following:

$$m_1 - m_3 = d \times A_{PS} \times \rho_{Si} \quad (2)$$

where d is the average depth of the porous silicon and A_{PS} is the front surface area of the porous silicon, as determined by SEM. The density of crystalline silicon, ρ_{Si}, is 2.33 g cm^{-3} [27].

The physical structure of the porous silicon depends upon etching condition. Control of pore diameter, depth and spacing is achieved by varying current density, etch time and wafer resistivity. After etching, the wafers are rinsed with methanol and water. The porous layer of the wafer is then coated with a 20 nm gold film via E-beam evaporation (Telemark 880). A schematic of the gold-coated porous silicon material is shown in Fig. 1c.

2.3. Electrochemical testing

The cycling of porous silicon has been examined using galvanostatic electrochemical techniques. The discharge–charge tests were performed at constant current using an electrochemical cell (HS Test cell, Hohsen Corp., Japan) with a multichannel BT2000 battery tester (Arbin Instruments BT2000, USA) equipped with MITSPRO (4.21). The porous silicon structure is used as a working electrode and lithium foil as a counter electrode. The backside of the porous silicon is coated with copper for better contact to the copper current collector. Fiber glass filter paper (Fisher Scientific) is used as a separator, wetted with an electrolyte. The electrolyte is 1.0 M $LiPF_6$ in 1:1 (w w^{-1}) ethylene carbonate: diethyl carbonate (Ferro Corporation). All cells were assembled in an Argon-filled glove box. The cells were charged–discharged at room temperature between the voltages of 0.1 V and 2 V vs. Li/Li+.

2.4. Removal of porous silicon after cycling

The porous silicon was removed from the bulk silicon after cycling in order to characterize the properties of the underlying support layer. After cycling, the front surface of the wafer is exposed to a piranha solution (H_2O_2, 30% (v/v) and H_2SO_4, equal volumes, Fisher Scientific) for 30 s. Profilometry was performed and the resulting thickness of the bulk silicon was measured to determine how much of the underlying support layer is removed.

3. Results and discussion

3.1. Gold coated porous silicon

We compared the cycling of our material with and without a gold coating for a sample consisting of pores with an average diameter of 1 micron, an average depth of 10 microns, area of 1 cm^2 and mass of 1 mg for the active porous silicon. As shown in Fig. 2, the material without the gold coating provides capacities of 500 mAh g^{-1} for the first cycle and then 76 mAh g^{-1} after the 10th cycle at a constant current of 50 μA cm^{-2}. These results are consistent with those observed by Shin and coworkers [21,22]. The same porous silicon material with a gold coating resulted in capacities of 1619 mAh g^{-1} for the first cycle and 2452 mAh g^{-1} after the 10th cycle at a higher current of 100 μA cm^{-2}. The porous silicon without the gold coating was unable to cycle at a higher constant current. The specific capacity of the sample with a gold coating was much greater than the uncoated sample. For example, in cycle 2 the specific capacity for the gold-coated sample is seven times more than that of the uncoated sample and this difference grows with increasing cycles. To compare the effect of the internal pores, a gold-coated, non-porous silicon sample was tested and resulted in a maximum capacity of 1 mAh g^{-1} before failing after 10 cycles at

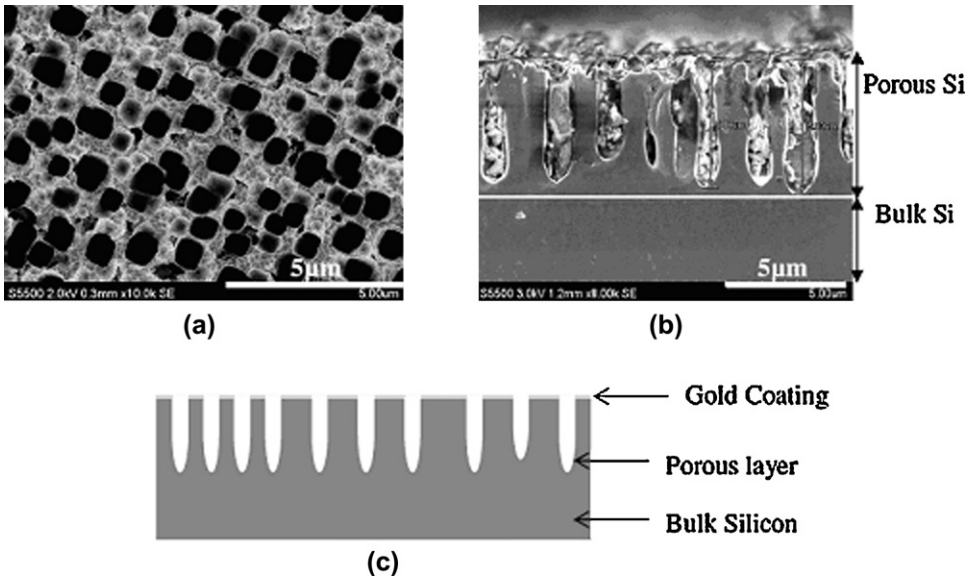

Fig. 1. A representative porous silicon sample (a) SEM top-view. (b) SEM cross-section view. (c) Schematic of cross-section, showing the bulk silicon, porous silicon, and thin gold coating.

0.25 mAh g^{-1} when cycled at a constant current of 100 μA cm^{-2}. We suspect that this enhanced electrochemical performance is due to both the internal pores and the gold coating, which creates a more stable interface between the electrolyte and the porous silicon electrode. Takamura et al. [28], showed that thin evaporated metal films enhanced the charge/discharge rates of graphite anodes. They proposed that metals such as gold and silver form a Li alloy and allow Li movement through the metal while providing a stable SEI interface between the carbon and the electrolyte. Fig. 3 compares the surface morphology of the porous silicon gold-coated and bare porous silicon after 10 cycles. The SEM images in Fig. 3a show that the non-coated porous silicon surface is severely cracked as compared to the gold-coated porous silicon. Lithium–silicon alloys (Li_xSi_y) are brittle, and combined with the large volume expansion in the material during lithiation, the non-coated porous silicon cracks to relieve internal stresses. There is no visual cracking or fragmentation observed on the gold-coated porous silicon electrode after ten cycles, shown in Fig. 3b. Only after 100 cycles, do we start to observe cracks in the gold-coated porous silicon. The gold coating hinders the structural degradation in the porous silicon as it undergoes volume expansion during lithiation. However, there is a gradual deterioration in the gold film caused by Li intercalation and deintercalation leading to loss in performance.

3.2. Electrochemical potential spectroscopy results

Electrochemical voltage spectroscopy was performed on a gold coated porous silicon sample containing pores with an average diameter of 1 μm, surface area of 0.72 cm^2, an average depth of 5.5 μm, and a porous silicon mass of 0.78 mg. The first cycle charge/discharge and the dC/dV vs. voltage plots are shown in Fig. 4. The anode is cycled between 0.1 and 2 V. Between these voltage limits, the capacity initially increases with each cycle, indicating that 0.1 V is below the lithiation potential of crystalline silicon leading to the lithiation of more and more crystalline silicon during every lithiation half-cycle. Obervac et al. has shown that the lower cutoff voltage should be above 0.05 V to remain in the two-phase region comprised of lithiated amorphous silicon and unlithiated crystalline silicon [29]. The voltage profile observed is consistent with previous Si studies [8,14,29–32]. During charging, region A in Fig. 4a and b, corresponds to the initial lithiation of the silicon, whereas the plateau shown by region B is a two phase region where

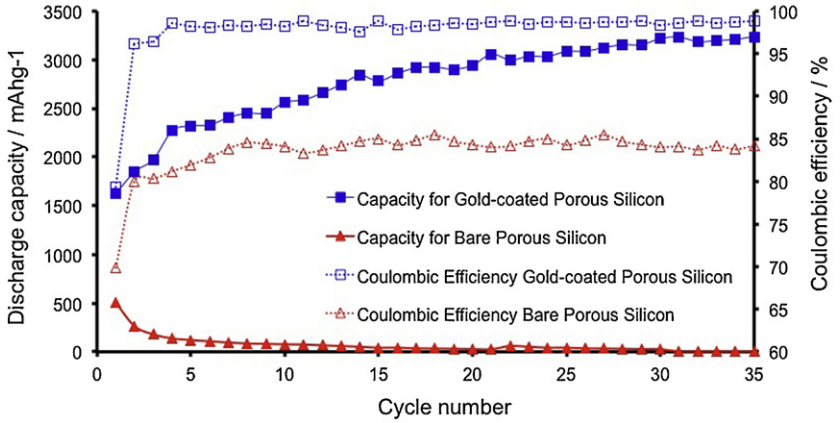

Fig. 2. Comparison of discharge capacity (filled symbols) and columbic efficiency (open symbols) vs. cycle number for gold-coated porous silicon (blue squares) and bare porous silicon (red triangles). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

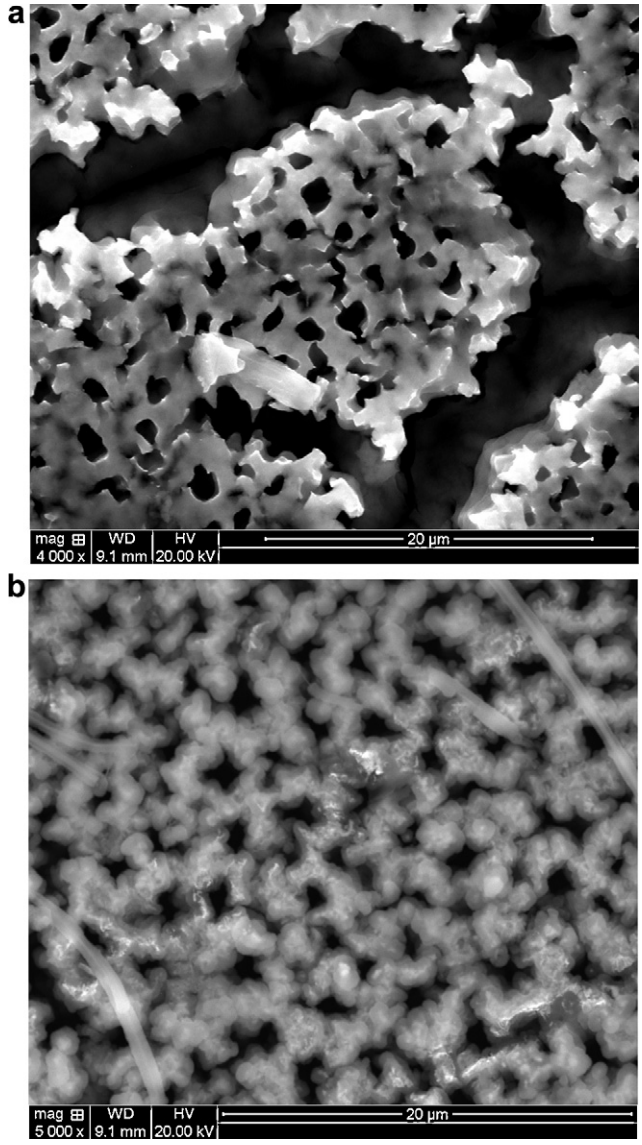

Fig. 3. SEM surface morphology of (a) non-coated porous silicon and (b) gold coated porous silicon electrode after 10th cycle of charge/discharge.

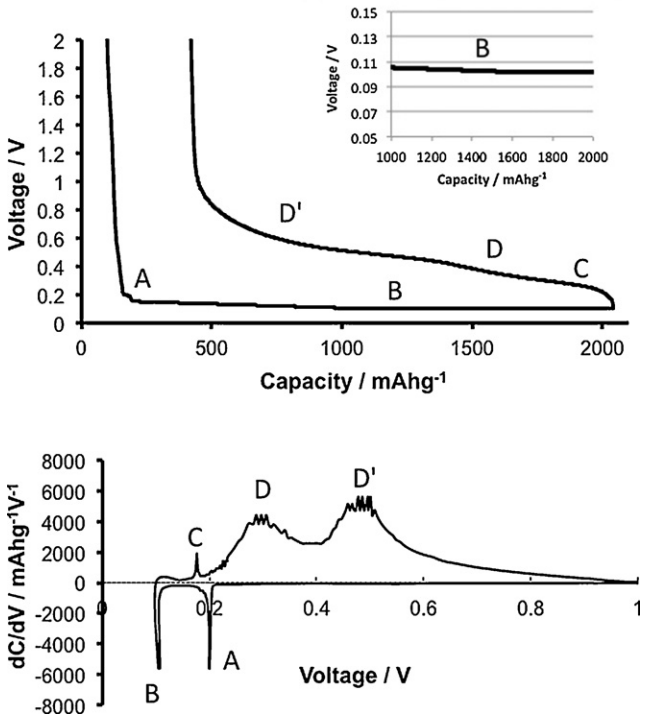

Fig. 4. Electrochemical potential spectroscopy data. (a) Voltage profile of the first cycle. Insert shows that region B remains constant. (b) Differential capacity curve of the first cycle.

crystalline Si is converted to an amorphous lithium silicide, a-Li_xSi [29]. The solid electrolyte interface (SEI) formation is thought to occur during the first cycle charge in the voltage range of 0.5–0.7 V [19], but no appreciable capacity peaks are observed in this region. During discharge, two broader peaks shown by regions *D* and *D′*, amorphous Li_xSi is converted to amorphous silicon.

A unique feature that is observed in our differential capacity curves in Fig. 4b is a peak at point C. The feature indicated by C is due to alloying of the 20 nm Au coating with lithium. Calculating the area under peak C results in a capacity of 10 mAh g^{-1} for the active material. If we consider only the mass of the Au film, this corresponds to 281 mAh g^{-1}-Au. Au is known to react with Li at low potential and has a capacity of 451 mAh g^{-1} for $Li_{15}Au_4$ [33,34]. Chan et al. [35] showed that a 50 nm film of Au resulted in an initial charge capacity of 47 mAh g^{-1}-Au at a rate of C/20. However, the charge/discharge capacity degrades quickly with increasing cycles.

Galvanostatic charge–discharge measurements at an initial constant current of 100 µA cm^{-2} (∼C/20) for 55 cycles, followed by a current of 150 µA cm^{-2} (∼C/15) for cycles 55–65, and 200 µA cm^{-2}(∼C/10) after the 65th cycle are shown in Fig. 5. The cell ran for 100 cycles with specific capacities over 2500 mAh g^{-1} (peaking at 3500 mAh g^{-1}) with columbic efficiencies over 97%. Upon increasing the C-rate, the specific capacity decreased with increasing cycles due to degradation in the material. Note that the mass used to calculate the capacity is the porous silicon mass. As will be later described, the bulk silicon does not appear to contribute to the lithiation and delithiation process.

As shown in Fig. 6a, the discharge voltage vs. capacity curves for various cycles reveal two discontinuities, *D* and *D′*, which corresponds to the low and high voltage delithiation respectively. Plateau *D* remains unchanged while plateau *D′* increases with each cycle, indicative of crystalline silicon converting to amorphous form. After cycle 55, when the charge–discharge rate is changed from 100 µA cm^{-2} to 150 µA cm^{-2} and eventually 200 µA cm^{-2}, plateaus *D* and *D′* becomes smaller resulting in a decreasing capacity with increasing cycles. As shown in Fig. 6b, each resulting cycle has a reduced capacity compared to the previous cycle and discontinuities begin to shift and become more pronounced. The reduction in *D′* indicates material degradation and eventual failure. Follow up experiments to examine the effect of C rate are underway.

There are obvious differences in the porous silicon structure before and after 163 cycles which can be seen via SEM, as shown in Fig. 7. Though there are pores visible in the porous silicon sample after cycling over 163 cycles, these visible pores are roughened and the smaller pores have disappeared. Though roughened, this structure was still producing specific capacities over 1000 mAh g^{-1}.

3.3. X-ray diffraction results

In additional to SEM, the structural changes in the porous silicon can be studied by X-ray diffraction (XRD, Rigaku Ultima II Powder XRD). XRD is based on measurement of the lattice spacing of crystallites which satisfy the Bragg condition for a particular reflection, therefore XRD can be used to evaluate the degree of crystallinity. We are able to remove the porous silicon from the bulk silicon via an acid wash step. Profilometer measurements after the wash step

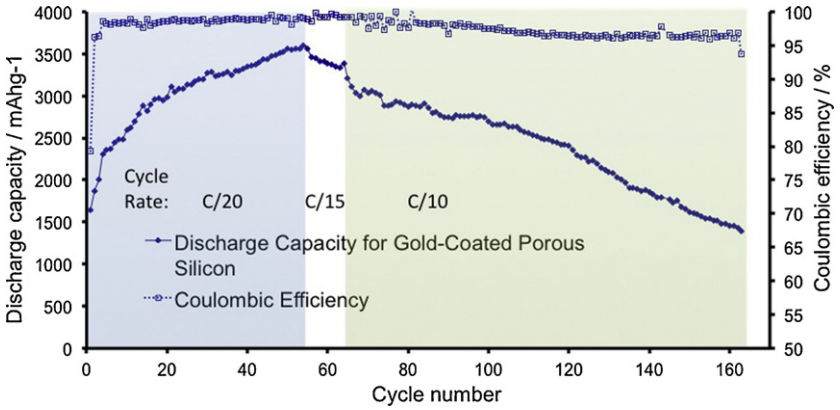

Fig. 5. Discharge capacity and efficiency vs. cycle number of the porous silicon anode during galvanostatic charge/discharge tested at 100 μA cm^{-2} (~C/20, shown in blue shaded region), 150 μA cm^{-2} (~C/15, shown in white shaded region), and 200 μA cm^{-2} (~C/10, shown in yellow shaded region) rates. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

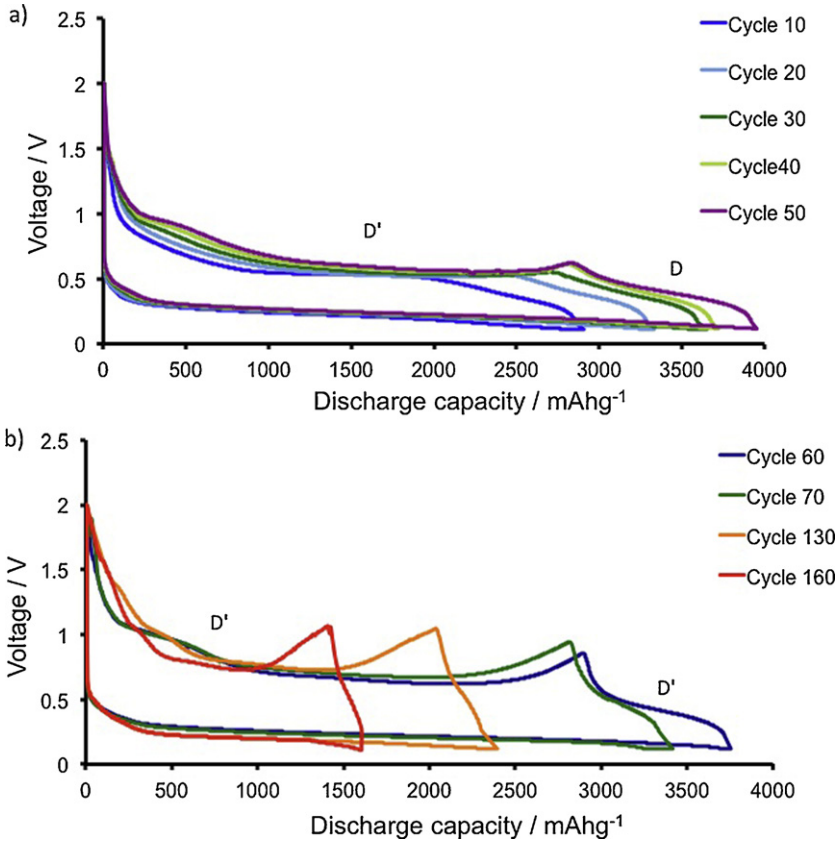

Fig. 6. Voltage vs. capacity profiles for (a) cycles 1–50 with capacity increasing with cycle number and (b) cycles 60–160 with capacity decreasing with cycle number. Plateau's *D* and *D'* corresponds to the low and high voltage delithiation, respectively.

resulted in a bulk silicon thickness of 294.1 ± 1.07 μm. This confirms that the porous silicon layer was removed entirely and that at most 1.47 microns of the support layer is removed. Interestingly, the bulk silicon shows two pronounced peaks that are characteristic of crystalline silicon after 163 cycles. An XRD pattern for native Si wafer (red), porous silicon before cycling (orange), porous silicon after 163 cycles (green) and silicon wafer after removing the lithiated/delithiated porous layer (blue)[1] is shown in Fig. 8. The two pronounced peaks in the XRD pattern for the native silicon wafer, the porous silicon before cycling, as well as the bulk silicon layer after cycling is characteristic of crystalline (1 1 1) silicon [17,36]. The porous silicon after cycling does not exhibit any sharp peaks, a characteristic of an amorphous structure. Other studies confirm that crystalline silicon becomes amorphous during lithium insertion [29]. Additionally, since the bulk silicon after cycling does not exhibit a structural change, we believe that it does not participate in the lithiation/delithiation process.

3.4. Error analysis of active silicon mass

For the above calculations, we calculate the discharge capacities based only on the porous silicon mass. If we consider that the 1.47

[1] For interpretation of the references to color in this text, the reader is referred to the web version of this article.

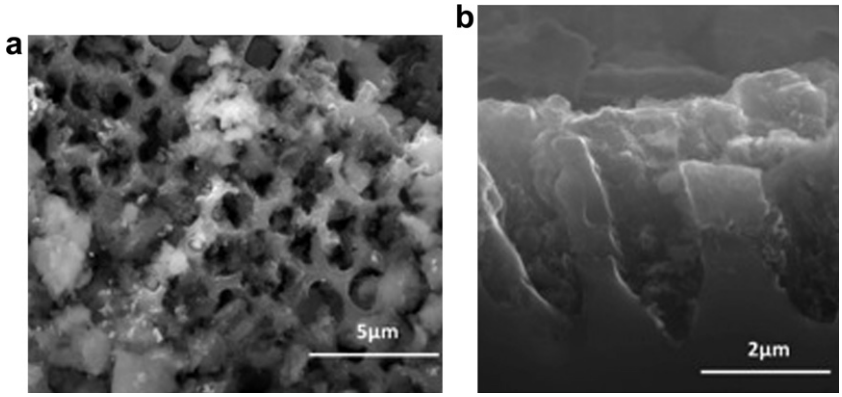

Fig. 7. (a) Top and (b) cross-section view of porous silicon after cycling with lithium for 163 cycles.

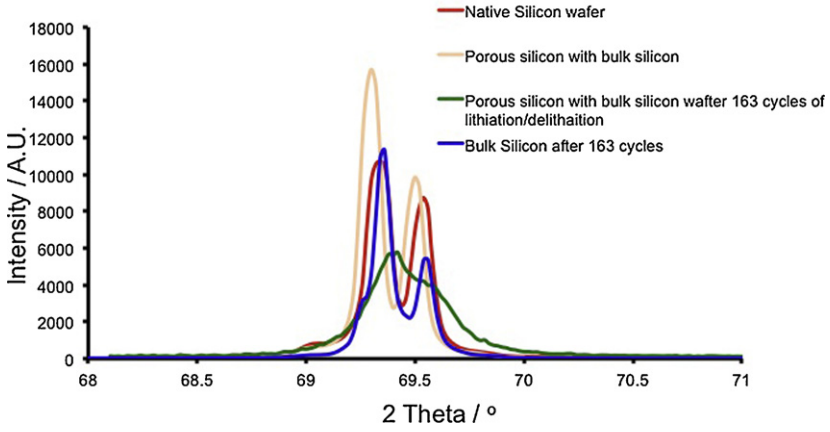

Fig. 8. XRD patterns comparing a bare silicon wafer and porous silicon before and after cycling with lithium.

micron support layer that may have been removed in our acid wash step did contribute to the lithiation process, our capacities would be 75.9% of that reported above. Instead of the max capacity of 3500 mAh g^{-1}, our max capacity would be 2659 mAh g^{-1}. Further examination of the interface between the porous silicon layer and the role of the support silicon layer are ongoing. The bulk silicon may play a role in alleviating in stresses generated in the porous silicon but it does not contribute significantly to lithiation.

4. Conclusions

A thin gold coating onto a porous silicon sample significantly enhances the capacity and cycleability of porous silicon. Our materials were able to achieve capacities over 1500 mAh g^{-1} for over 163 cycles. Structural evidence suggests that the porous silicon undergoes a phase transformation from crystalline silicon to amorphous silicon while leaving the bulk silicon support as crystalline silicon. Further studies elucidating the role of the gold and whether another material can be substituted for the gold are ongoing. Additionally, this structure can be fabricated using processing steps that are compatible with modern thin film processing techniques for easy scale up for lithium-ion batteries.

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